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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/681,327	03/19/2001	Jack Robert Smith	BUR920000098US1	9570

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EXAMINER	
VO, TED T	

ART UNIT	PAPER NUMBER
2122	5

DATE MAILED: 08/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No. 09/681,327	Applicant(s) SMITH ET AL.	
	Examiner Ted T. Vo	Art Unit 2122	

-- The MAILING DATE of this communication appears on the cover sheet with th correspond nc address --

P riod for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to the application filed on 03/19/2001.

Claims 1-20 are original claims.

Claims 1-20 are pending in the application.

Claim objections

2. Claims 2-8, 10-14, 16-20 are objected to. Underlined words are used for amending claim limitations in a marked-up version. The claims 2-8, 10-14, 16-20 are original claims. The words in the claims would be used as standard format and not be underlined. Correction in accordance to MPEP 714 is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-20 are rejected under 35 U.S.C. 102(a) as being anticipated by Chow et al., "PipeRench Implementation of the Instruction Path Coprocessor", IEEE, Dec. 2000.

Given the broadest reasonable interpretation of followed claims in light of the specification.

As per claim 1:

Regarding claim limitation: ***"A data processing system, comprising: a central processing unit (CPU)*** (figure 1, page 149, core processor) ***in communication with a system m mory; legacy code stored in said memory*** (figure 1, page 149, Object code)***, where said legacy code is not optimized fro that CPU; a code-optimizing coprocessor*** (figure 1, page 149, Instruction Path coprocessor) ***in communication with said system memory and said CPU; and said control logic within said code-optimizing coprocessor that causes said code-optimizing coprocessor to generate*** (figure 1, page 149, backed-arrow, modified instructions) ***optimized code*** (figure 1, page 149, modified code) ***from said legacy code wile CPU is executing said legacy code, such that said optimized code is tailored to said CPU*** (see abstract and see page 148, section 2.1.1, 'runs concurrently with core processor').

-Chow discloses an architecture (figure 1) which comprises a core processor (CPU) in communication with a memory (figure 1, page 149, Object code). The coprocessor generates optimized code (figure 1, page 149, Instruction Path coprocessor) from object code. The optimized code is stored within the memory that stores the object code. It allows the core processor to use the optimized code with a new format that can be more efficiently executed (see abstract).

As per claim 2: Chow teaches the coprocessor that is used for modifying object code (legacy code) into modified code (optimized code); the modified code is restored in memory and utilized by the core processor (CPU) (see page 147, second column, lines 1-2; see page 150, second column last paragraph).

As per claim 3: Chow teaches the coprocessor that comprises a fill buffer and data memory (see page 151, figure 5) linking together. The page-table entry (claim limitation) operation is inherent from a common pipeline, where this operation must fit into sizes of hardware elements.

As per claim 4: The program counter is inherent in processor architecture, since every processor which implements a memory, a cache or an array must contain a counter. And the function of a counter is to point at an instruction or data that is used by a processor. According to figure 1, it shows the modified code and the object code stored in the memory for being fetched by the core processor; therefore, it

inherently teaches that the optimized code is utilized in lieu of at least some of the object code (legacy code).

As per claim 5:

Chow discusses the L1 cache and L2 Cache as parts of processor hardware for storing fetched instructions (see page 154, first column, section 4.1).

As per claim 6: Chow shows the coprocessor that generates the optimized code and stores the code in the near area of object code (see figure 1).

As per claim 7: Control logic is in the coprocessor since the coprocessor is a hardware element.

As per claim 8: Chow teaches inherently the control logic comprising software because coprocessor is programmable (see abstract). The coprocessor includes I-COP code that is modifiable for controlling the coprocessor without hardware changing (see page 147, second column, second paragraph).

As per claim 9: Claim 9 is a method that utilizes the coprocessor to optimize the legacy code in accordance to the claim 1. The claimed functionality corresponds to the functionality of claim 1; therefore the claim is rejected in the same reason as set forth in connecting to the rejection of claim 1.

As per claim 10: Claim 10 is a method that utilizes the coprocessor to optimize the legacy code in accordance to the claim 2. The claimed functionality corresponds to the functionality of claim 2; therefore the claim is rejected in the same reason as set forth in connecting to the rejection of claim 2.

As per claim 11: Claim 11 is a method that utilizes the coprocessor to optimize the legacy code in accordance to the claim 3. The claimed functionality corresponds to the functionality of claim 3; therefore the claim is rejected in the same reason as set forth in connecting to the rejection of claim 3.

As per claim 12: Claim 12 is a method that utilizes the coprocessor to optimize the legacy code in accordance to the claim 4. The claimed functionality corresponds to the functionality of claim 4; therefore the claim is rejected in the same reason as set forth in connecting to the rejection of claim 4.

As per claim 13: Claim 13 is a method that utilizes the coprocessor to optimize the legacy code in accordance to the claim 5. The claimed functionality corresponds to the functionality of claim 5; therefore the claim is rejected in the same reason as set forth in connecting to the rejection of claim 5.
As per claim 14: Claim 14 is a method that utilizes the coprocessor to optimize the legacy code in accordance to the claim 6. The claimed functionality corresponds to the functionality of claim 6; therefore the claim is rejected in the same reason as set forth in connecting to the rejection of claim 6.

As per claim 15: Claim 15 is a data processing system that utilizes the coprocessor to optimize the legacy code in accordance to the claim 1. The claimed functionality corresponds to the functionality of claim 1; therefore the claim is rejected in the same reason as set forth in connecting to the rejection of claim 1.
As per claim 16: Claim 16 is a data processing system that utilizes the coprocessor to optimize the legacy code in accordance to the claim 2. The claimed functionality corresponds to the functionality of claim 2; therefore the claim is rejected in the same reason as set forth in connecting to the rejection of claim 2.
As per claim 17: Claim 17 is a data processing system that utilizes the coprocessor to optimize the legacy code in accordance to the claim 3. The claimed functionality corresponds to the functionality of claim 3; therefore the claim is rejected in the same reason as set forth in connecting to the rejection of claim 3.
As per claim 18: Claim 18 is a data processing system that utilizes the coprocessor to optimize the legacy code in accordance to the claim 4. The claimed functionality corresponds to the functionality of claim 4; therefore the claim is rejected in the same reason as set forth in connecting to the rejection of claim 4.
As per claim 19: Claim 19 is a data processing system that utilizes the coprocessor to optimize the legacy code in accordance to the claim 5. The claimed functionality corresponds to the functionality of claim 5; therefore the claim is rejected in the same reason as set forth in connecting to the rejection of claim 5.
As per claim 20: Claim 20 is a data processing system that utilizes the coprocessor to optimize the legacy code in accordance to the claim 6. The claimed functionality corresponds to the functionality of claim 6; therefore the claim is rejected in the same reason as set forth in connecting to the rejection of claim 6.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kothari et al., US No. 6,339,840.

Dunn et al., US No. 6,314,560

Chow et al., "Instruction Path Coprocessors", ACM, May 2000.

Patel et al., "rePLay: A Hardware Framework for Dynamic Program Optimization", CiteSeer, December 1999.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (703) 308-9049. The examiner can normally be reached on Monday-Friday from 8:00 AM to 5:30 PM ET. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam, can be reached on (703) 305-4552.

The fax phone numbers for this Group are:

Official: (703) 746-7239; After Final: (703) 746-7238; Non-Official: (703) 746-7240.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

TUAN Q. DAM
PRIMARY EXAMINER

TTV
August 7, 2003